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| EXAMINER | |
|---|---|
| THOMAS, SHANE M | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/643,577 | FAANES ET AL. | |
| | Examiner | Art Unit | |
| | SHANE M. THOMAS | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *7,8,14,15,22,24,25 and 29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,8,14,15,22,24,25 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/28/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office action is responsive to the amendment filed 1/28/2008. Claims 7,8,14,15,22,24,25, and 29-32 are pending. Applicants' arguments and amendments to the claims have been carefully considered, but they are not persuasive and do not place the claims in condition for allowance. Accordingly, this action has been made FINAL.

All previous outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

### *Information Disclosure Statement*

The information disclosure statement filed 1/28/2008 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the reference of Kohn, J.R. appears to have an incorrect patent number (7,243,211) associated with the reference. As such, the reference has been crossed out and the remainder of the IDS considered. A signed copy has been attached herewith.

### *Response to Amendment*

Applicant's amendments to the claims have overcome all outstanding rejections. Upon further consideration, the Examiner has cited the prior art references of Hughes, Henry, Hennessy, and Yamahata (all previously cited) to teach the presently amended claims.

The amendment to claim 29 has resulted in an indefinite issue.

The amendment to claims 31 and 32 has resulted in a new matter issue as discussed below.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 31 and 32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claims 31 and 32, support for the newly amended limitations of the first queue "monitoring scalar memory requests to the higher level cache" and the second queue "monitoring scalar memory requests that are serviced by the higher level cache but not yet written to the local cache" cannot be found in Applicant's originally-filed specification; therefore, the claims contain new matter.

Page 17, lines 21-28, of Applicant's original specification states that the logical division of the FOQ results in a first queue for accesses to the DCache (e.g. a "local cache") and the second queue is for accessed to the ECache (e.g. a "higher level cache"). As such, the claimed methods of use for the queues are not described in the specification in such a way to make or use the invention.

Claims 29-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 29, it is not clear which FOQ the term --the FOQ-- is referring (lines 13,19,21,25, and 26) as the claim sets forth a plurality of FOQ - one included with each cache controller of the plurality of cache controllers (line 4). Nonetheless, for the purposes of examination, the Examiner has considered the terms --the FOQ-- to be any of the FOQs of the cache controllers.

Claims 30-32 are rejected as being dependent upon a rejected base claim.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7,8,22,24,25, and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes (U.S. Patent No. 6,393,536) in view of Henry et al. (U.S. Patent Application Publication No. 2003/0018875) in further view of Hennessy et al. (*Computer Organization and Design: The Hardware / Software Interface*).

As per claim 7, Hughes teaches **a computerized method for accessing data in a memory system having a local cache** (data cache 28) **and a higher level cache** (optional L2 cache - [10/53-55] **comprising:**

**obtaining a memory** [14/20-24];

**storing the memory request in an Initial Request Queue (IRQ) -** LS1 cache buffer 60 - figure 3.

**processing the memory request from the IRQ by a cache controller** [15/1-5], **wherein processing includes:**

**determining whether the memory request hits in the local cache** (data cache 28 - figure 6, step 152)**;**

**determining whether a portion of an address associated with the memory request matches one or more addresses in a Forced Order Queue (FOQ),** LS2 buffer 62, [18/18-24], [19/58-62] and/or miss address buffer - [17/39-60]. Because the address of an incoming request is compared to each entry of the MAB [17/41-52] and the LS2 buffer [19/58-62], it follows that each portion of the address associated with the incoming request is checked against the address portion of the MAB and the LS2 buffer entries to determine whether the addresses match. Thus if the multiple portions (thereby comprising the whole address) of an incoming request's address are compared to determine a match, a single portion would therefore have to be compared as well, as multiple single portions of an address comprise an entire address.

**wherein the FOQ stores a memory request that is pending to the higher level cache** (L2 cache can fill requests that miss data cache 28 - [17/44-45]) and can hold entries that miss data cache 28 - [17/6-8].

Hughes does not specifically teach the portion of an address associated with a memory request matching one or more partial addresses in a FOQ. Henry teaches a store forwarding method (figure 3) that initially compares the index portion of a load address (Step 306) against a pending store's index. Figure 2 shows that the index 204 is a partial address of physical address 188. By comparing only page index in parallel with the TLB lookup, instead of waiting until after the TLB determination to see if the load request address matches a store address in the store buffer ¶31, a reduction in the instruction latency is achieved by reduction in the number of pipeline stages required (¶16). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the invention of Hughes with the teachings of Henry in order to have decreased the memory request latencies of accessing the FOQ (LS2 buffer 62) of Hughes. Store forwarding as taught by Henry could and replaced or improved the store forwarded of Hughes as taught in [19/26+].

Hughes further teaches:

**if the portion of an address associated with the memory request does not match the one or more partial addresses in the FOQ** (figure 6, step 150) **and, at the same time, the memory request hits in the local cache** (figure 6, steps 152)**, servicing the memory request immediately using data in the local cache** (figure 6, step 156)**;** Hughes teaches that the steps of 150 (checking the incoming request address against the LS2 addresses) and the steps of 152-156 (checking the incoming request address against the data/local cache) can occur is parallel (e.g. at the same time) - [26/9-13];

**if the portion of an address associated with the memory request does not match the one or more partial addresses in the FOQ and, at the same time** [26/9-13]**, the memory**

**request misses in the local cache** (figure 6, steps 150,152,154) **, adding the memory request to the FOQ** [26/26-27] Hughes does not specifically teach **allocating a cache line in the local cache corresponding to the local cache** miss; however, such operation is well known in the art of caching. Hennessy teaches on page 606 ("Queston 3") that a decision regarding which cache line to remove from the cache, and thereby allocate for the new cache line that is requested, occurs for a cache miss. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the memory system of modified hughes with the well known allocation technique of Hennessy in order to have added the requested cache line to the cache by allocating an entry in the cache, thereby increasing the temporal locality of the request. Hughes also teaches **servicing the memory request using data received from the higher level cache** (L2 cache can be used to retrieve data missed in a lower level cache as known in the art - [17/44-45]**; and**

**if the portion of an address associated with the memory request matches the one or more partial addresses in the FOQ** (figure 6, step 150)**, preventing the memory request from being satisfied in the local cache** (step 158 to 162 to figure 7, step 170 to step 178 {as the SLIF bit was set in step 162 of figure 6}, to step 172 to step 176 {the prevention of satisfying the request from the local cache can be seen as occurring in steps 172 and 176}**, wherein preventing includes adding the memory request to the FOQ** (figure 6, step 162) **and servicing the memory request using data received from the higher level cache** (data can be received from the L2 cache if a miss occurs to the data cache 28 as known in the art - [17/44-45]).

As per claim 8, Hughes teaches **obtaining a memory load or a memory store request** [16/17-18].

As per claim 22, the rejections follows the rejection for claim 7 set forth above. Hughes further teaches a **cache controller** (combination of logic circuits 64 and 66) **having a FOQ** (combination of miss address buffer and LS2 buffer).

As per claim 24, Hughes teaches that in one specific implementation of the present embodiment of the invention, the data cache 28 comprises an address generator (address translation circuitry) to generate one or more physical addresses from the one or more addresses of the scalar load/store command [17/20/23]; however, Hughes does not specifically teach the address generator being a part of load/store unit 26. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the load/store unit 26 of Hughes by implementing the address translation circuitry as part of the load/store unit 26 instead of the data cache, since it has been held that rearranging parts of an invention involves only routine skill in the art. Refer to MPEP § 2144.04(vi): Such a modification would have increased the speed in which translated addresses are written into the LS2 buffer by not having to send the translated physical address across the address bus 80 [17/34-37].

As per claim 25, Hughes teaches wherein the address generator (address translation circuitry) generates the one or more physical addresses using a translation look-aside buffer (TLB) [17/27-31].

As per claim 29, the rejection follows the rejection for claims 7 and 22 set forth above with one modified interpretation. As per claim 29, Hughes inherently teaches a plurality of cache controllers (as Hughes shows multiple processor and L2 combinations in figure 13) -

[32/47-55], **wherein each cache controller includes a FOQ** (because, the processor L2 combinations may be identical [32/47-55], it could have been seen that two FOQ would have been present in the system of figure 13).

As per claim 30, Hughes teaches **wherein the FOQ includes a FOQ index array** (the Examiner is considering dependency link file 104 (figure 4) to be the index array) **wherein the FOQ index array contains a copy of indices** (Data Store Tags, which are also contained in the LS2 buffer [16/64-65], that are dependent on load tags are stored in dependency link file 104) **and control information** (the Load Instruction Tag for the corresponding Data Store Tag) **for the FOQ entries** - [20/53 - 21/12].

As per claims 31 and 32, because the LS2 buffer 62 (a portion of the FOQ) contains both pending requests to the higher level cache (e.g. requests that miss the data cache 28 - figure 6, step 150) and memory requests that are serviced by the higher level cache but not yet written to the data cache (e.g. load requests that have hit the L2 cache but are in flight to be stored to the data cache 28) - [16/61-65], it would have been obvious to one having ordinary skill in the art to have modified the FOQ of Hughes to logically divide the FOQ into these first and second queues as such a logical division of a resource would require only routine skill in the art as discussed in MPEP §2144.04 (see sections of "Making Separable" and "Re-arrangement of Parts").

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes (U.S. Patent No. 6,393,536) in view of Henry et al. (U.S. Patent Application Publication No. 2003/0018875) in further view of Hennessy et al. (*Computer Organization and Design: The Hardware / Software Interface*), as applied to claim 7 above, in further view of Yamahata (U.S. Patent No. 5,247,639).

As per claim 14, Hughes teaches a multiprocessing system in figure 13 and [32/47-56] with processors 10 and 10a independently connected to the bus bridge 202 for connection to main memory 204. Hughes does not specifically teach processing the memory request in the FOQ when local when local cache processing is bypassed. Yamahata teaches a cache bypass bit for use when multiple processors are to obtain synchronization by using semaphore data in [2/4-38]. Specifically Yamahata teaches in [2/15-19] that an instruction decoder sends a bypass request to a bus control unit to bypass a local cache. Hughes shows a bus interface unit 37 connected to the load/store unit 26 in figure 2. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the multiprocessing system of Hughes with the cache bypassing during multiprocessor synchronization teaching of Yamahata in order to have been able to maintain a level of cache coherency between the processors 10 and 10a of modified Hughes when both processors would be attempting to update main memory 204. The utilization of semaphore data instructions are well known in the art to be utilized in multiprocessing systems for contention of a shared resource (in the case of Hughes, it would be main memory 204).

As per claim 15, the rejection follows the rejection of claim 14, supra. Local cache processing is bypassed when the memory request includes a synchronization request (i.e. via a

cache bypass bit 801 - [7/23-35]). The memory request can be seen to be a synchronization request since the bypass bit would be set in a memory request when attempting to access semaphore data to attain synchronization between the multiple processor 10 and 10a of modified Hughes 10 and 10a [2/35-38 Yamahata.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed whose telephone number is (571) 272-4188. The Examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Shane M. Thomas/
Patent Examiner

21 April 2008

/Pierre-Michel Bataille/
Primary Examiner, Art Unit 2186
April 21,2008